International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-2566

January 2017
VOLUME-1
ISSUE-1
Page:7916-20

Implementation of a Low Power FIFO based BIST Process for CUT

1.B. KISHORE BABU1, 2.V. NAGA RANI2
1PG Scholar, Dept of ECE, DVR & Dr. HS MIC College of Technology, Kanchikacherla, AP, India,
2Assistant Professor, Dept of ECE, DVR & Dr. HS MIC College of Technology, Kanchikacherla, AP, India,

Abstract: The on line transparent test technique for detection of latent hard faults which develop in first input first output buffers of routers during field operation of NOC and also propose fault tolerant solution by introducing shared buffer in router. It provides alternative way in case of detection of faults otherwise used to improve efficiency. The technique involves repeating tests periodically to prevent accumulation of faults. NOC approach has emerged as a promising solution for on chip communications. The test technique utilized by the test hardware tries to incorporate the advantages of both parallel and serial approaches of testing embedded memories, thereby reducing the test time. For the test architecture proposed in the thesis, a test scheduling algorithm has been focusing on limiting the number of concurrent test blocks under power constraint with the aim of performing a power aware test of the memory cores. The scan chain reordering technique is the major criteria for the reduction of Power.
Keywords: NOC, FIFO, Scan Chain Reordering, Line Transparent Test Technique.

I.INTRODUCTION

Over a last decade years, network-on-chip has been improved communication infrastructure compared with bus-based communication network for different types of networks on a chip designs appears the difficulties related to bandwidth, signal integrity, and power dissipation. However, like all additional systems-on-a-chip (SOCs), NOC-based SOCs must be tested for errors and defects. Testing the circuits and elements of the networks on chip infrastructure contains testing routers and inter-router links. Mostly the amount of area of the NOC data transport medium is occupied by the routers, which is most part occupied by routing logic and FIFO buffers. Consequently, the probabilities of run-time defects or faults occurring in buffers and logic are mostly higher compared with the other components in the circuit of the NOC. Hence, test process for the NOC communication infrastructure must begin to test of routing logic and buffers of the routers. In addition, the test must be performed repeatedly in certain intervals of time to ensure that no error or fault gets accumulated. The random run-time functionality errors or faults have been one of the major concerns during testing of severely scaled CMOS-based memories. These errors or faults are a result of physical effects, such as environmental susceptibility, low supply voltage, aging and hence are alternating (non-permanent indicating device damage or malfunction) in nature. Though, these intermittent errors or faults regularly show a relatively high occurrence rate and in time have a tendency to become permanent faults. Additionally, wear-out of memories also effect intermittent faults to become frequent enough to be classified as permanent faults. Hence, there is a need for on-line test technique that can identify the run-time faults, which are intermittent in nature but slowly become permanent fault over time. Chip combination has reached a stage wherein a complete system and all circuits of oil can be placed on a single chip. When we say complete system, we mean all the required elements that make up a specialized kind of application on a single silicon substrate material. This integration has been made possible because of the fast developments in the field of VLSI designs. This is primarily used in embedded systems. Thus, in simple terms a SOC can be defined as an Integrated Circuit (IC), designed by stitching together multiple stand-alone VLSI designs to provide full functionality for an application

II. FIFO BASED SYSTEM

A. Transparent Test Generation

The faults considered in this brief, if applied for SRAMs or DRAMs, can be detected using standard March tests. However, if the same set of faults are

International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-2566

January 2017
VOLUME-1
ISSUE-1
Page:7916-20

considered for SRAM type FIFOs, March test cannot be used directly due to the address restriction in SRAM type FIFOs mentioned in and thus we were motivated to choose single order address MATS ++ test (SOA MATS ++) for the detection of faults considered in this brief. The word oriented SOA MATS ++ test is represented as {_ (wa) ; ↑ (ra,wb) ; ↓ (rb, wa) }; _ (ra) } where, a is the data background and b is the complement of the data back ground ↑ And↓ are increasing and decreasing addressing order of memory, respectively.

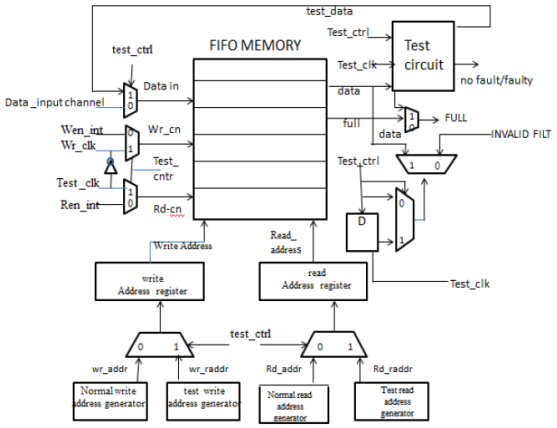

Fig.1. Basic Architecture of FIFO based BIST

It means memory addressing can be increasing or decreasing. Application of SOA MATS ++ test to the FIFO involves writing patterns into the FIFO memory and reading them back. However, online memory test techniques require the rebuilding of the memory contents after test. Thus, researchers have modified the March tests to transparent March test so that tests can be performed without the requirement of external data background and the memory contents can be restored after test. We have thus transformed the SOA MATS ++ test to transparent SOA MAT S ++ (TSOA MATS ++) test that can be applied for online test of FIFO buffers.

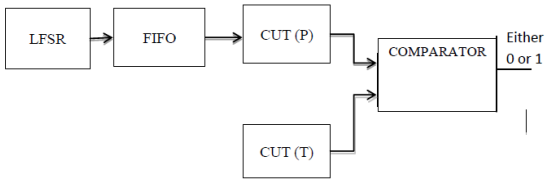

Fig.2. Block diagram of FIFO based BIST process.

Algorithm: Transparent Soa-Mats++ Test

N= number of rows of the FIFO memory
i ← 0;
while(i ≤ N-1) **do**
j ← 0;
while(j≤2) **do**
temp←read (i);
if(j = 0) **then**
original← temp;
write (i, !temp);
else
if(j = 1) **then**
result ← compare(temp,original);
write(i,!temp);
end if
else
Result ← compare(temp,original);
end if
j ← j+1;
end while
i ← i+1;
end while

Assume a stuck At 1 fault at the most significant bit (MSB) position of the word stored in LUT. Thus, instead of storing 0101, it actually stores 1101 and as a result, the stuck at fault at the MSB gets excited. During the second iteration of j, when LUT is readdressed, the data read into temp is 1101. At this point, the data p resent in temp and \ original are compared (bitwise XOR). An all 1's pattern is expected as result. Any 0 within the pattern would mean a stuck at fault at that bit position as shown in Fig.2.

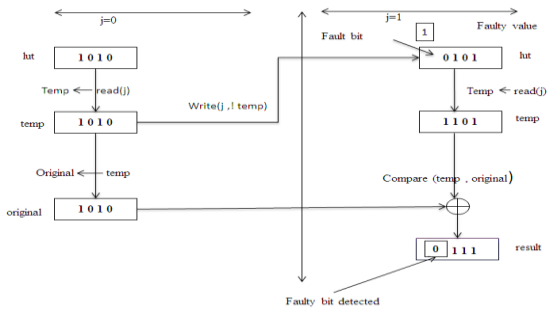

Fig.3. Fault Detection ofInvert and Restore Phase of Transparent SOA-MATS++ Test.

International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-2566

January 2017
VOLUME-1
ISSUE-1
Page:7916-20

Where the XOR of 1010 and 1101 yields a 0 at the MSB position of the result indicating a stuck-at-fault at the MSB position. However, for cases where the initial data for a bit position is different from the faulty bit value, the stuck-at-fault cannot be detected for the bit position after the re-store phase of the test. It thus requires one more test cycle to excite such faults.

B. Scan Chain Reordering

In VLSI design for testability, a scan chain is commonly used to connect the shift registers that store the input and output vectors during the testing phase of manufacturing. Registers in the scan chain are connected as a single path with ends of the path connected to a primary input (PI) pad and a primary output (PO) pad. Test input values are shifted into the registers through the PI pad; then, a test is performed and the test output values are shifted out through the PO pad. Fig.3 depicts a simple example of a scan chain.

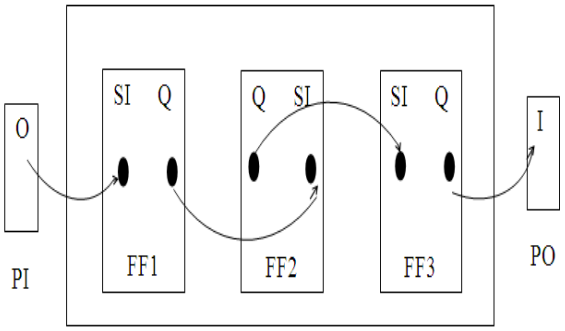

Fig.4. scan chain re-ordering block diagram.

One of the primary objectives in design-for-testability is to minimize the impact of test circuitry on chip performance and cost. Thus, it is essential to minimize the wire length of a scan chain this decreases wiring congestion and/or reduces the chip area while, at the same time, increasing signal speed by reducing capacitive loading effects on nets that share register pins with the scan chain. Previous placement-based scan chain ordering approaches compute the cost of stitching one flip-flop to another as either cell-to-cell.

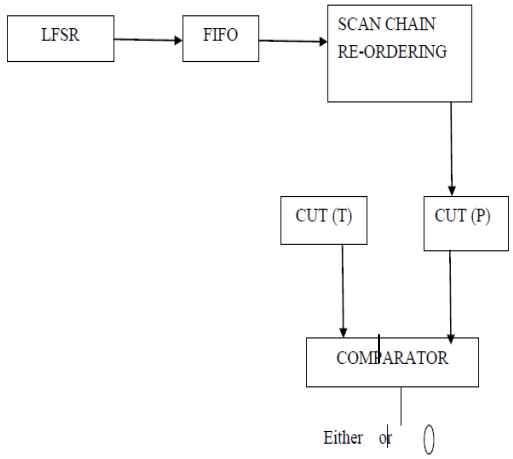

Fig.5. FIFO Based BIST Process with Scan Chain re-ordering technique.

After the scan chain re-ordering technique is applied to the circuit then the circuit is verifying by using the comparator to find out the fault or error is present or not the process is as shown in above the Fig 5.

III. SIMULATION RESULTS

Results of this paper is as shown in Fig.5 and 6.

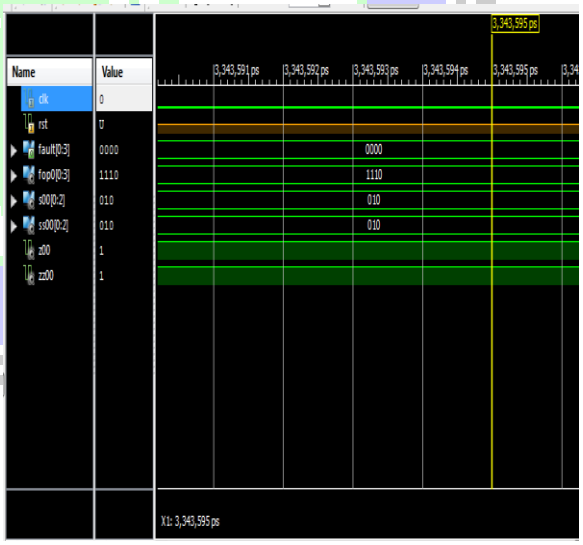

Fig.6.FIFO based BIST process using scan chain re-ordering without error

International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-2566

January 2017
VOLUME-1
ISSUE-1
Page:7916-20

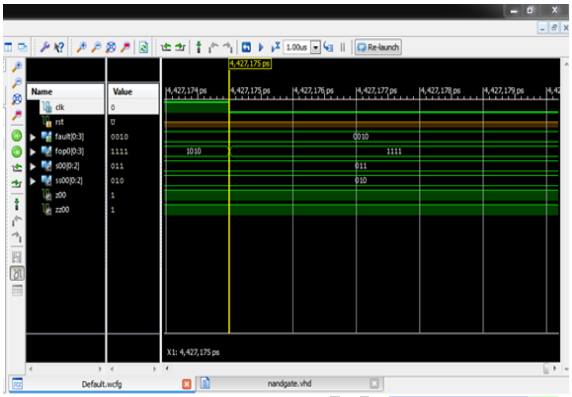

Fig.7.FIFO based BIST process using scan chain re-ordering with error

In the FIFO based BIST process the total power utilized is 0.181watt (181 mw). The power analysis of this project will be shown in the Fig.7.

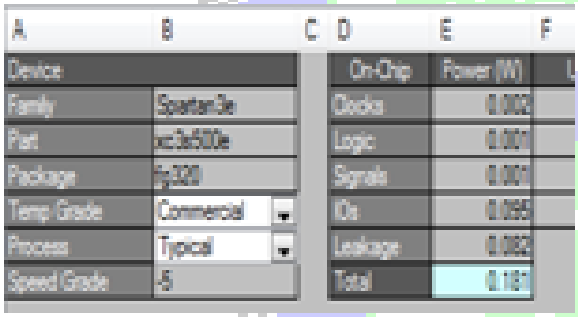

Fig.8.Power utilization of FIFO based BIST process

In the FIFO based BIST process when the Scan Chain Re–ordering technique is applied the total power utilized is 0.092watt (92 mw). The power analysis of this project will be shown in the Fig.9.

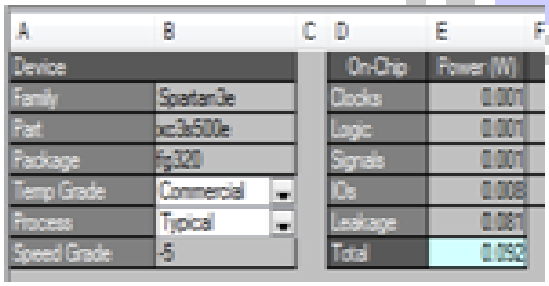

Fig.9.Power utilization of FIFO based BIST processusing Scan Chain Re-ordering technique

IV. EXPERIMENTAL RESULTS

The simulation is performed on XILINX ISE14.5 software; result ofsimulation includes parameters such as power dissipation, delay. The comparison of this project and before existing methods the power will be reduced up to 50% as shown in below Fig.8.

Para meters	Existing method	Proposed method	Difference in %
Time	31.658 nS	31.332 nS	1.1% Reduced
Power	0.181 W 181 mW	0.092 W 92 mW	49% Reduced

Fig.10.Comparison of Existing System and Proposed System

V. CONCLUSION

In this paper, A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak powers are substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

VI. REFERENCES

[1]BibhasGhoshal, Kanchan Manna, SantanuChatto-padhyay, and IndranilSengupta, “In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers,” IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 24, NO.1 pp.393-397.,2016.

[2]A. M. Amory, C. Lazzari, M. Lubaszewski, and F. G. Moraes. A New Test Scheduling Algorithm Based on Networks-on-Chip as Test Access Mechanisms. Journal of Parallel Distributed Computing, 71(5):675–686, 2011.

[3]P. Bernardi, M. Grosso, M. Reorda, and Y. Zhang.A Programmable BIST for DRAM Testing and Diagnosis. In Proceedings of International Test Conference, pages 1 10,November 2010.

[4] S. Bahl and V. Srivastava.Self-Programmable Shared BIST for Testing Multiple Memories.In 13th European Test Symposium (ETS), pages 91 –96, May 2008.

[5]L. Benini and G. D. Micheli. Chapter 1 - Networks on Chip.In Networks on Chips,pages1–22. Morgan Kaufmann, San Francisco, 2006.

[6] .Borri, M. Hage-Hassan, L. Dilillo, P. Girard, S. Pravossoudovitch, and A. Virazel.Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test. Journal of Electronic Testing, 21(2):169–179, April 2005.

[7]R. Aitken. A Modular Wrapper Enabling High Speed BIST and Repair for Small Wide Memories. In Proceedings of International Test Conference, pages 997– 1005, October 2004.

[8]A. Benso, S. Di Carlo, G. Di Natale, P. Prinetto, and M. Bodoni. Programmable Built-in Self-Testing of Embedded RAM Clusters in System-on-Chip Architectures. Communications Magazine, IEEE, 41(9):90–97, September 2003.

[9] R. D. Adams. High Performance Memory Testing: Design Principles, Fault Modeling and Self-Test. New York, USA, 2002.

[10]M. Bushnell and V. Agrawal.Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits.Springer, 2000.

[11] Various Methods of DRAM Refresh. In Technical Note TN-04-30. Micron Technology, Inc., 1999.

[12] A. Bondavalli, S. Chiaradonna, F. D. Giandomenico, and F.Grandoni.Threshold-Based Mechanismsto Discriminate Transient from Intermittent Faults. IEEE Transaction onComputers, 49(3):230–245, 1998.

[13]S. Barbagallo, M. L. Bodoni, D. Medina, G. de Blasio, M. Ferloni, F. Fummi, and D. Sciuto. A Parametric Design of a Built-in Self-Test FIFO Embedded Memory. In Proceedings of the Workshop on Defect and Fault-Tolerance in VLSI Systems (DFT'96),pages221–229, 1996.

Author's Profile:

Mr. Bethala Kishore Babucompleted his B.Techin P.V.P Siddhartha Institute of technology and perceiving M.tech from D.V.R &Dr HS MIC college of technology . He attended for many wok shops, international seminars and got a an excellence in them.

Mrs.Vasantha Naga Rani, currently working as Assistant Professor in ECE Department at D.V.R &Dr HS MIC College of Technology. Her research and her enthusing interests include high-performance development at her college applications.