

NEW ISOLATED MULTILEVEL INVERTER BASED ON CASCADED THREE-PHASE CONVERTER BLOCKS

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ABSTRACT— This paper displays another topology of an isolated multilevel inverter that can be utilized for high voltage and high power applications, for example, coordinating battery stockpiling system and elective vitality sources to power network. With reduced number of segments the proposed fell multilevel inverter requires one and only dc source by falling high frequency transformers. The center building hinders in the multilevel inverter are the six-switch three-stage converters that are controlled using PWM stage moved plan for symphonious reduction. Discussions have been given to contrast the proposed cascaded multilevel inverter and run of the mill existing fell inverters. Simulation and correlation examines have been completed to verify the execution of the proposed multilevel inverter. Index Terms- Cascaded converter, isolation, multilevel inverter, single DC source, three-phase converter.

I INTRODUCTION

To address the perpetually expanding interest for vitality and the earnest ecological effect issues brought on by human activities identified with vitality creation and utilization, one of the most encouraging arrangements is to jolt transportation for enhanced fuel productivity and lessened outflow, and to implement perfect, renewable vitality frameworks for electricity generation on a huge scale with high entrance. The marketshare of electric drive vehicle (EDV) in the US has been increasing relentlessly from 0.14% of new auto deals in 2011 to 0.72% in 2014 [1], which could achieve a more critical level of infiltration sooner rather than later. Renewable Portfolio Standards (RPS) [2] went in a larger part of states in the U.S. and the new fuel proficiency models of a normal fueleconomy of 35.5 miles for every gallon (mpg) by 2016 [3] providesupports in approach to Batteries have been distinguished by the DOE as one of the critical advancements for EDVs that incorporate cross breed electric vehicles (HEVs), module crossover electric vehicle (PHEVs), and battery electric vehicles (BEVs) [4]. A surge of resigned EDV batteries will be seen as more EDVs hit

the road, identified as the empowering advances to accommodate renewable sources into future force systems (e.g., Smart Grids, Microgrids, or their mix with conventional power systems) [8]. Sandia National Laboratories discharged a report on the specialized and economic feasibility of such methodologies quite a long while back [5]. However, management of huge scale battery stockpiling systems, particularly with utilized EDV batteries, is exceptionally testing task and likewise requires more research on force electronic converters and control methods. Multilevel inverters have gotten to be workhorse in grid connected applications at medium and/or high voltage levels because by and large it is difficult to interface a solitary power semiconductor change straightforwardly to the brace [18]. These technologies are utilized to furnish power with low cost, reduced all out consonant twisting (THD), lessened dv/dt, optimal size, and low electromagnetic impedance (EMI) without disseminating a lot of force [9-18]. In general, multilevel inverter topologies can be grouped into four main groups: 1) diode-clipped, otherwise called unbiased point clamped (NPC) inverters; 2) capacitor clamped inverters (moreover called flying capacitor inverters); 3) fell H-bridge multilevel inverter with discrete dc sources; and 4) interconnected three stage inverters, for example, Hexagram converter [13, 15, 16, 18]. Additionally, different sorts of topologies have likewise rose, for example, the one that is executed by means of falling the essential structures called hybrid inverters [9, 11, 18]. A decent synopsis on different multilevel converters can be found in [16]. The diodes in a NPC inverter clasp the voltage and the capacitors at the yield are in arrangement to share the high voltage. As an outcome, every switch stands just with one capacitor voltage [16]. Be that as it may, the inverter experiences capacitor unbalance voltage issue and unfavorably huge number of cinching diodes when the quantity of voltage level is substantial [15]. Likewise, the reverse recuperation of clasping diodes turns into a noteworthy design challenge if the inverter

keeps running under heartbeat width modulation(PWM) for high-voltage high-control applications [18] H-span module will need to manage throbbing power.2"(a the Hexagramconverter not appropriate for huge battery stockpiling framework thatrequire power administration on every battery module.This paper displays another topology of a fell multilevelinverter for high voltage and high power applications such asgrid associated battery stockpiling frameworks and other alternative2energy sources to power network. With lessened number ofcomponents the proposed fell multilevel inverterrequires one and only dc source by falling high frequencytransformers. Entrenched control techniques can be usedfor this multilevel converter. The PWM stage moved plan, an exceptionally prevalent technique in modern applications, is utilized forthe proposed inverter to lessen the sounds in the outputvoltage. Reproduction and examination ponders have been carriedout to check the execution of the proposed inverter.

II. CASCADED TRANSFORMERS TOPOLOGIES WITH ONE DC SOURCE

The cascaded multilevel inverter becomes one of the mostsingle dc power voltage source. This construction is used topile output voltage levels up by increasing number oftransformers instead of increasing number of dc voltagesources. Moreover, the HBCT inverter provides filtering effectof harmonic components due to the leakage reactance thecascaded transformers [9] and also provides electric isolationbetween output and source [13].In the HBCT inverter, the primary terminals of the transformers winding are connected to the H-bridge inverters to synthesize output voltage of $+V_{dc}$ 0 V and $-V_{dc}$ while the terminals of the secondary winding are connected in series toelevate the output voltage. The amplitude of the output voltage is determined by the turn ratios of the cascaded transformersand the input dc voltage. Hence, this inverter can operate ineither symmetric or asymmetric modes to synthesize steps of output voltage [9]. The maximum number of phase voltage levels in a symmetric HBCT inverter is given by: $m=2K+1$ (1)where m, K are number of voltage levels and number of cascaded transformers, respectively. The output voltage can be obtained by summing the voltages across the secondary terminals of the cascadedtransformers. $V_o = L \cdot \frac{dV_k}{dt}$ (2) synthesize steps of output voltage [9]. The maximum number of phase voltage levels in a symmetric HBCT inverter synthesize steps of output voltage [9]. The maximum number of phase voltage levels in a symmetric HBCT inverter

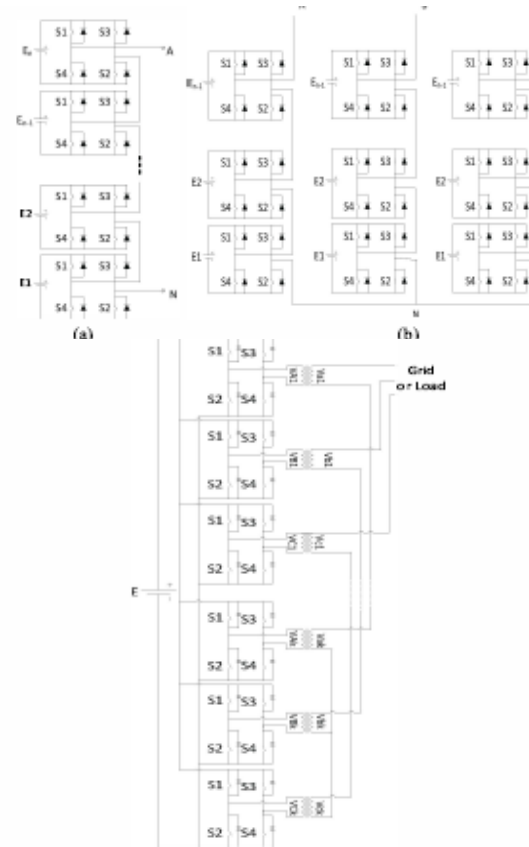


Fig. 2. Topology of a three phase H-bridge cascaded transformer (HBCT) multilevel inverter [17]

III. PROPOSED SIX-SWITCH CASCADED TRANSFORMERMULTILEVEL INVERTER

A new cascaded transformer based multilevel invertertopology with one single dc source is proposed in this paper.The building blocks in the proposed multilevel inverter are six-switch three phase inverters, not the single phase H-bridgeconverters used in the HBCT shown in Figs. 1 and 2. Fig. 3shows the initial circuit topology of the six-switch cascadedtransformer (SSCT) multilevel inverter, based on which thenew topology will be developed. One of the advantages ofusing three-phase converters as building blocks is that dqframe based control can be used, which is simpler and canto the primary terminals of a high frequency transformer togenerate three voltages at the output side: $+V_{dc}$, 0 V and $-V_{dc}$.The two inverters are controlled by a 12-pulse

PWM technique (unipolar PWM drive technique of three-phase inverter) where the upper inverter is driven by the first 6 pulses while the remaining pulses are used to control the second inverter. The pulses are generated by comparing a triangular carrier waveform with two sinusoidal modulating waves for each phase which are of the same magnitude and frequency but 180° out of phase. For example, pulses 1, 2, 7 and 8 are used to drive the corresponding switches which are connected to phase A where S2 and S5 are complementary switches for S1 and S7, respectively. As a result, S1 and S5 work together to perform +V_{dc} and 0 while S2 and S7 are used to provide -V_{dc} and 0 at output terminals. In other words, the two inverters work together as a complementary device for each other, making it easy to connect them to three single-phase high frequency transformers.

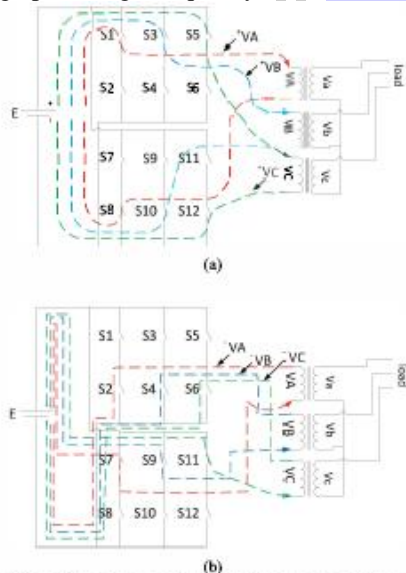


Fig. 4. Basic cell of the proposed inverter in the initial circuit topology: (a) three phase positive level, and (b) three phase negative level.

Well established carrier based PWM modulation techniques (such as phase-shifted or level-shifted modulation) for multilevel inverter can be used for the SSCT inverter. In this paper, the phase-shifted scheme, a very popular method in industrial applications, is used to control the SSCT inverter to reduce harmonics in the output voltage [15]. All the six-switch building blocks are connected to the same dc source in parallel and all secondary terminals of the basic units are connected in series to elevate the output voltage. As a result, the voltage level is increased by cascading more

transformers. The peak of the output voltage is determined by the turn ratios of the cascaded transformers, the number of voltage levels and the input dc voltage. The SSCT inverter can operate in either symmetric or asymmetric mode. If all the turn ratios are the same, the inverter is known as symmetric multilevel inverter and the resulting output ac voltage could swing from $+K_a V_{dc}$ to $-K_a V_{dc}$ where K_a are the number of the cascaded transformers and the turn ratio, respectively. The output phase voltage can be determined by summing the voltages across the secondary terminals of the cascaded transformers, which can be described by (2) as well. The number of phase voltage levels in the symmetric SSCT inverter. It is noticed that the proposed SSCT inverter acts similarly to the three phase HBCT multilevel inverter while the proposed inverter has ability to reduce the number of semiconductor switches. One six-switch inverter block in the last stage in the cascaded string can be removed. Moreover, in the other stages, certain six-switch inverter blocks can be removed as well. For the other stages (other than the last stage), one six-switch block can be removed for each stage except one stage that still needs to have two inverter blocks to provide a complementary path (e.g., block A'B'C' in Fig. 5(b)) for all the remaining six-switch inverter blocks, as shown in Fig. 5 (b). The transformer at the last stage can be removed if electric insulation is not needed and this shows a nine-level SSCT inverter of its initial version with 8 six-switch inverters while Fig. 5(b) shows the compact SSCT inverter with only requirements, size and manufacturing cost.

IV. SIMULATION AND COMPARISON STUDIES

In multilevel inverter topologies, number of system components normally has a proportional relationship with the number of output voltage levels. Increased number of system components will increase the size of inverter, weight and cost and also imposes higher requirement of insulation and complicates the control.

Moreover, these drawback factors will challenge system reliability by means of the voltage level goes up. So, as discussed earlier, a new inverter topology is proposed to have more output voltage levels with less system components. Table I presents the number of components required to implement a nine-level inverter with different topologies including the proposed inverter. The proposed inverter achieves a 36% reduction in the number of system components required and uses only thirty switches compared to symmetric converter under resistive load.

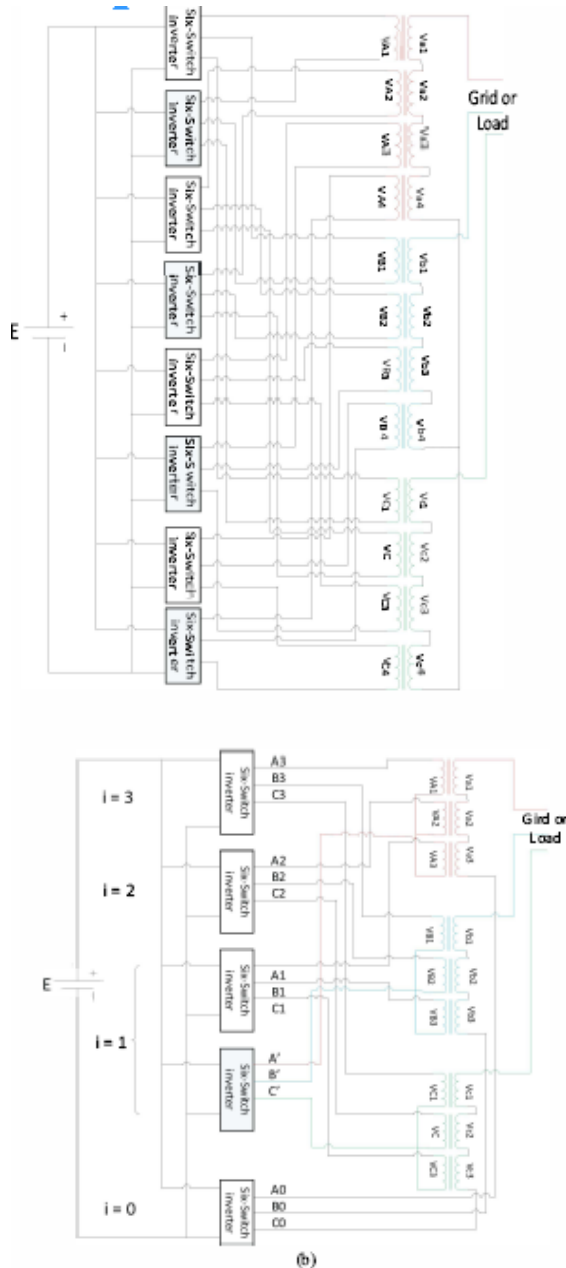


Fig. 5. The proposed inverter: (a) The initial SSCT inverter, (b) The compact SSCT inverter with component number reduced.

TABLE I
COMPARISON OF TOTAL COMPONENT REQUIREMENT FOR A NINE-LEVEL
INVERTER UNDER DIFFERENT TOPOLOGIES.

	Cascaded H-bridge [18]	HBCT inverter [12]	CHBCT inverter [13]	Sub- Multilevel inverter [9]	Proposed inverter
Trans- formers	0	4	4	2	3
Switches	48	48	36	36	30
dc source	12	1	1	2	1
Diodes	48	48	36	36	30
Total #	108	101	77	76	64
% of reduction	0%	6.5%	28.7%	29.6%	40.7%

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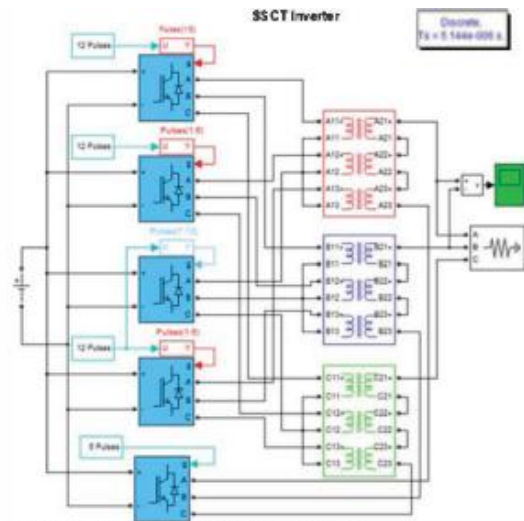


Fig. 6. The compact SSCT inverter simulation system.

fig. 7 and 8 show the output voltage waveforms and the corresponding THD% for both the proposed and the HBCT multilevel inverters. The carrier frequency is set to 1080 Hz and the high frequency transformers also have the same rated frequency. The result shows that the traditional topology still has better performance in THD%. Nevertheless, it is interesting to note that the proposed inverter has smaller low order (below 16th) harmonic components though the total THD% is higher. It is relatively easier to filter high frequency harmonics than low order ones. As shown in Figs. 7(b) and 8(b), the output THD% of the proposed inverter is close to the HBCT with a 0.5 kVar capacitive load added.

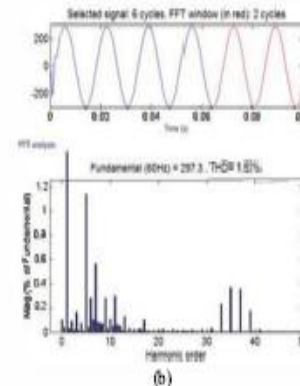


Fig. 8. Output voltage waveforms of the HBCT inverter: (a) Output voltage without filtering; and (b) Output voltage with 0.5 kVar capacitor.

V. CONCLUSION

This paper presents a new topology of isolated multilevel inverter which has a single dc source with the help of cascaded high frequency transformers. The proposed isolated multilevel inverter consists of three phase six-switch converters with reduced number of power components compared with the existing topologies. The proposed inverter can be used for high voltage and high power applications such as grid connected battery storage and alternative energy systems. Using three-phase converters as building blocks enables dq-frame based simple control and eliminates the issues of single phase pulsating power, which can cause detriment to a limit on certain dc sources. Simulation studies have been carried out to compare the proposed multi-level inverter with an H-bridge cascaded inverter. The simulation results verified the performance of the proposed inverter. Though the proposed topology does not show advantage in reducing the total amount of harmonics, the lower order of harmonics in the proposed inverter have been significantly reduced, which makes it easier to filter out high order harmonics.

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