International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-256

September 2016
VOLUME -2
ISSUE-5
Page:7926-30

BUILT IN GENERATION OF FUCNCTIONAL BROADSIDE TESTS USING A FIXED HARDWARE STRUCTURE

1.MD.SADDAM,2. M.SHOBAN BABU
1. PG Scholar, Dept of ECE, Anubose Institute of Technology, Palwancha, khammam 2. Dept of ECE, Anubose Institute of Technology, Palwancha, khammam

ABSTRACT: This project described an on-chip test generation method for functional broadside tests. The hardware was based on application of primary input sequences in order to allow the circuit to produce reachable states. Random primary input sequences were modeled to avoid repeated synchronization and thus yield varied sets of reachable states by implementing a decoder in between circuit and L.F.S.R. Two-pattern tests were obtained by using pairs of consecutive time units of the primary input sequences. The on-chip generation of functional broadside tests required simple hardware and achieved high fault coverage for testable circuits. Further, power can be reduced by using bit swapping LFSR. This technique yields less number of transitions for all pattern generation. Bit-swapping technique is less complex and more reliable to hardware miscommunications. C17,s27,ALU tests are performed in this concept.

KEYWORDS: BIST, reachable states, on-chip, L.F.S.R, fixed hardware architecture, broad side test, decoder.

INTRODUCTION:

Technology provides smaller, faster and lower energy devices which allow more powerful and compact circuitry, however, these benefits come with cost-the nano scale devices may be less reliable, thermal-and shot- noise estimations alone suggest that the fault rate of an individual nanoscale device may be orders of magnitude higher than today's devices. As a result, we can expect combinational logic be susceptible to faults. So in order to test any circuit or device we require separate testing technique which should be done automatically, for that purpose we are going to BIST. In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been intro- duced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern.

LITERATURE SURVEY:

However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation [1]. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation [1]–[3]. Several techniques that have been developed to reduce the peak and average power dissipated during scan-based tests can be found in [4] and [5]. A direct technique to reduce power consumption is by running the test at a slower frequency than that in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time [6]. Furthermore, it fails in reducing peak-power consumption since it is independent of clock frequency. Another category of techniques used to reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scanchain-ordering techniques [7]–[13]. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture). The design of low-transition test-pattern generators (TPGs) is one of the most common and efficient techniques for low-power tests [14]–[20]. These algorithms modify the test vectors generated by the LFSR to get test vectors with a low number of transitions. The main drawback of these algorithms is that they aim only to reduce the average-power consumption while loading a new test vector, and they ignore the power consumption that results while scanning out the captured response or during the test

International Journal of Engineering In Advanced Research Science and Technology ISSN: 2278-256

September 2016
VOLUME -2
ISSUE-5
Page:7926-30

cycle. Furthermore, some of these techniques may result in lower fault coverage and higher testapplication time. Other techniques to reduce average-power consumption during scan-based tests include scan segmentation into multiple scan chains [6], [21], test-scheduling techniques [22], [23], static compaction techniques [24], and multiple scan chains with many scan enable inputs to activate one scan chain at a time [25]. The latter technique also reduces the peak power in the CUT. OVERTESTING due to the application of two-patternscan-based tests was described in [1]–[3]. Over testing is related to the detection of delay faults under non-functional operation conditions. One of the reasons for these non-functional operation conditions is the following. When an arbitrary state is used as a scan-in state, a two-pattern test can take the circuit through state-transitions that cannot occur during functional operation. As a result, slow paths that cannot be sensitized during functional operation may cause the circuit to fail [1].

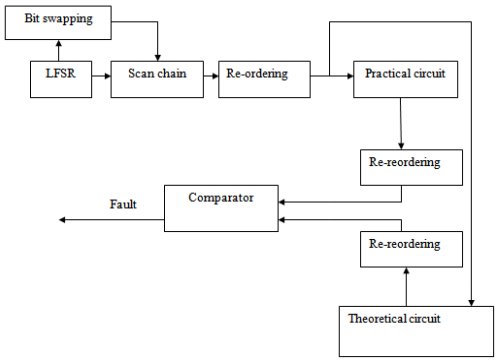
BIST: BUILT IN SELF TEST:

The trend to include more test logic on an ASIC has already been mentioned. Built-in self-test (BIST) is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. In each case the principle is to generate test vectors, apply them to the circuit under test (CUT) or device under test (DUT), and then check the response. BIST is a viable approach to test today's digital systems. With the ever increasing need for system integration, the trend today is to include in the same VLSI device a large number of functional blocks, and to package such devices, often, in Multi-Chip Modules (MCMs) that comprise complex systems. This leads to difficult testing problems in the manufacturing process and in the field**.** An attractive approach to solve these problems is to use a multi-level integrated Built-In Self-Test (BIST) strategy**.** This strategy assumes that BIST is used at each level of manufacturing test, and it is reused at all consecutive levels, i.e. device, MCM, board, system. Boundary-Scan standard to realize self-testing at different levels. This strategy can only be realized.

Galois LFSR:

Named after the French mathematician Évariste Galois, an LFSR in Galois configuration, which is also known as **modular**, **internal XORs** as well as **one-to-many LFSR**, is an alternate structure that can generate the same output stream as a conventional LFSR (but offset in time). In the Galois configuration, when the system is clocked, bits that are not taps are shifted one position to the right unchanged. The taps, on the other hand, are XOR'd with the output bit before they are stored in the next position. The new output bit is the next input bit. The effect of this is that when the output bit is zero all the bits in the register shift to the right unchanged, and the input bit becomes zero.

The bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions**.** The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG. In the BS-LFSR, consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4$, $cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced.



CIRCUIT UNDER TEST:

ISCAS 89 benchmark circuits: Digital electronics is classified into combinational logic and sequential logic. Combinational logic output depends on the inputs levels, whereas sequential logic output depends on stored levels and also the input levels.The memory elements are devices capable of storing binary info. The binary info stored in the memory elements at any given time defines the state of the

sequential circuit. The input and the present state of the memory element determine the output. Memory elements next state is also a function of external inputs and present state. A sequential circuit is specified by a time sequence of inputs, outputs, and internal states. **ISCAS** was Initiated in 1968, by a small group of distinguished circuit theorists, IEEE ISCAS has grown into a premier annual conference reflecting the diversity, richness, and significance of the circuits and systems fields, as well as the growing technological applications and knowledge economy that is based on circuits and systems fundamentals. It is the largest yearly conference under IEEE Circuits and Systems Society, which attracts thousands of hundreds of researchers throughout the world. ISCAS is frequently considered an "academic" conference, whose participants are predominantly researchers in universities. Unlike its sister conferences such as ISSCC, DAC and ITC, it gets less number of industry attendance and industry papers.

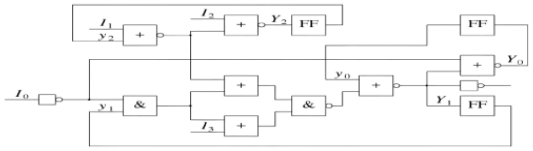


Fig1: s27 Sequential

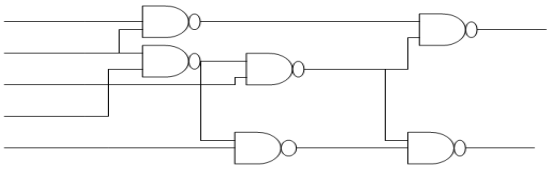


Fig2:c17

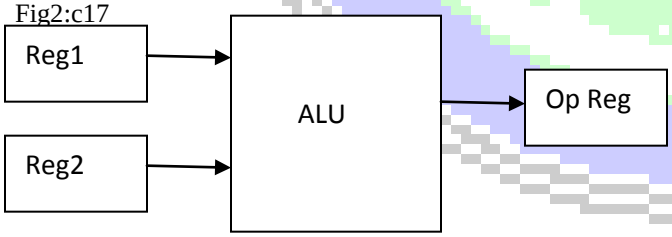


Fig3: ALU Block diagram

ALGORITHM

Step1: Start

Step2: Apply pattern to the BS-LFSR by reset-1.

Step3: Run by reset-0 and activate the clock.

Step4: Apply BS-LFSR output to scan chain.

Step5: The output patterns of scan chain are re-ordered using cell re-ordering algorithm.

Step6: Apply these patterns to the theoretical and practical circuits.

Step7: The output of these circuits is again re-ordered.

Step8: The re-ordered outputs of both circuits are compared to each other by using comparator.

Step9: If the fault is present in the circuit, the comparator shows its output as 1.

Step10: If there is no fault in the circuit, the comparator shows its output as 0.

Step11: Stop.

All above steps are applied to drawn circuits for S27, C17, and ALU as shown in above figures.

IMPLEMENTATION:

XILINX:

Xilinx, Inc. (NASDAQ: XLNX) is the world's largest supplier of programmable logic devices, the inventor of the field programmable gate array (FPGA) and the first semiconductor company with a fabless manufacturing model

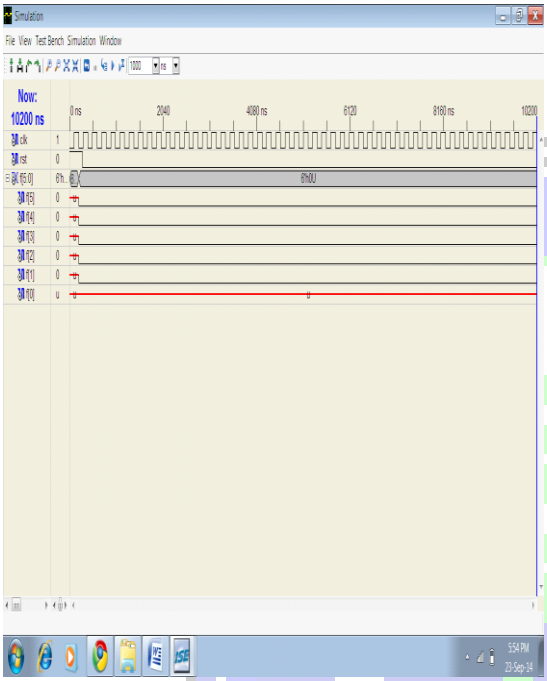
IN the Xilinx software we can do simulation and synthesis .The entire processor will be implemented using the Xilinx FPGAs so you won't have to spend time wiring up that part of the circuit. You will, however, have to wire the switches and lights that are used to control the processor, and have to wire the Xilinx part itself to the switches and lights, but this shouldn't be too bad. You will also use the backplane bus in your lab kit so that the Triscuit will be built on two boards: one for the Xilinx chip, and one for the switches and lights.

The HDL Editor feature provides extensive edit and search capabilities with language-specific color coding of keywords, as well as integrated on-line syntax checking to scan verilog code for errors. The Language Assistant feature speeds design entry by providing a lookup list of typical language

constructs and commonly used synthesis modules like counters, accumulators, and adders.

SIMULATION:

WITH FAULT:



c

CONCLUSION: This paper presents a low hardware overhead TPG for scan- based BIST that can reduce switching activity in CUTs during BIST and also achieve very high fault coverage with a reasonable length of test sequence with fixed hardware architecture. Unacceptably long test sequences are often required to attain high fault coverage with pseudo- random test patterns for circuits that have many random pattern resistant faults. C17, S27, ALUs are implemented with lowpower BIST using bit swapping LFSR. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits. While this objective still remains important, reducing heat dissipation during test application is also becoming an important objective. Since the correlation between consecutive patterns applied to a circuit during BIST is significantly lower, switching activity in the circuit can be signicantly higher during BIST than that during its normal operation. Excessive switching activity during test application can cause several problems.

REFERENCES:

[1] J. Rearick, "Too Much Delay Fault Coverage is a Bad Thing", in Proc. Intl. Test Conf., 2001, pp. 624-633.

[2] J. Saxena, K. M. Butler, V. B. Jayaram, S. Kundu, N. V. Arvind, P. Sreeprakash and M. Hachinger, "A Case Study of IR-Drop in Structured At-Speed Testing", in Proc. Intl. Test Conf., 2003, pp. 1098-1104.

[3] S. Sde-Paz and E. Salomon, "Frequency and Power Correlation between At-Speed Scan and Functional Tests", in Proc. Intl. Test Conf., 2008, Paper 13.3, pp. 1-9.

[4] J. Savir and S. Patil, "Broad-Side Delay Test", IEEE Trans. On Computer-Aided Design, Aug. 1994, pp. 1057-1064.

[5] I. Pomeranz, "On the Generation of Scan-Based Test Sets with Reachable States for Testing under Functional Operation Conditions",in Proc. Design Autom. Conf., 2004, pp. 928-933.

[6] Y.-C. Lin, F. Lu, K. Yang and K.-T. Cheng, "Constraint Extraction for Pseudo-Functional Scan-Based Delay Testing", in Proc. Asia and South Pacific Design Autom. Conf., 2005, pp. 166-171.

[7] Z. Zhang, S. M. Reddy and I. Pomeranz, "On Generating Pseudo-Functional Delay Fault Tests for Scan Designs", in Proc. Intl. Symp. on Defect and Fault Tolerance in VLSI Systems, 2005, pp. 398-405.

[8] I. Polian and F. Fujiwara, "Functional Constraints vs. Test Compression in Scan-Based Delay Testing", in Proc. Design, Autom. and Test in Europe Conf., 2006, pp. 1-6.